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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,152	09/16/2003	Andrew Lines	FULCP006	8727

22434 7590 04/04/2007

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,152	LINES ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2006 and 12 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☒ Claim(s) *22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-49 have been considered. Claims 1, 14-16, 21, 27, 28, 31, and 49 have been amended as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment filed 12 October 2006 and Amendment filed 12 January 2007.

Claim Objections

3. Claims 22 and 44 are objected to because of the following informalities: Taking claim 1 as exemplary, please change the claim language from "At least one computer-readable medium having data structures stored therein representative of the circuit of claim 1" to --At least one computer-readable medium having data structures stored therein representative of ~~the circuit of claim 1~~ **an asynchronous circuit...**", where the "..." symbolizes the rest of the language from claim 1. This is to remove the ambiguity whether claims 22 or 24 are independent or dependent claims and the scope of the claim language within claims 22 and 24. Applicants made similar amendments to claims 27 and 48 in the Amendment filed 12 January 2007. The suggested corrections are also to maintain consistency among the claim language styles. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 23-26 and 45-48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification mentions in a total of three sentences on page 16, paragraph 0050 implementing the device in simulatable representation. However, there are hundreds of methods and ways to implement the current circuit and system within software in a simulator with netlists and hardware description language. Without a specific description of how the circuit and system is to be implemented within software in a simulator, a person of ordinary skill in the art would require an extraordinary amount of undue experimentation to correctly implement the circuit and device via these specific methods, e.g. within a software simulator with netlists and/or HDL.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-14, 20, 22, 27-32, 34-35, 37-42, 44, and 49 are rejected under 35 U.S.C. 102(b) as being taught by Vegesna et al., U.S. Patent Number 5,488,729 (herein referred to as Vegesna).

8. Referring to claims 1, 22, and 27, taking claim 1 as exemplary, Vegesna has taught an asynchronous circuit for processing units of data having a program order associated therewith (Vegesna column 8, lines 17-26), the circuit comprising

a. An N-way-issue resource comprising N parallel pipelines (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 27-37; column 12, line 55 to column 13, line 15; Figure 13; column 15, lines 11-23; Figure 15; column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; and Figure 24),

b. Each pipeline being operable to transmit a subset of the units of data in a first-in first-out manner (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 17-37; column 12, line 55 to column 13, line 15; Figure 13; column 14, lines 53-61; Figure 14(b); column 15, lines 11-23; and Figure 15),

c. Issuance of the data units in the respective pipelines being staggered in time (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 17-37; column 12, line 55 to column 13, line 15; Figure 13; column 14, lines 53-61; Figure 14(b); column 15, lines 11-23 and 43-54; and Figure 15 – In regards to Vegesna, while the instructions are fetched simultaneously, the individual pipelines themselves control the issuance of the instructions and data, so there is only a possibility that the instructions will be issued by the individual pipelines simultaneously. The issuance of the instructions are dependent upon whether the dependency of the instruction is resolved or not, so an individual pipeline would stall an instruction's issuance to a later point in time when the instruction dependency has been resolved. Also, pipelines themselves stagger the issuance of instructions in individual pipelines, since the individual pipelines issue its instructions at different points in time, as shown in Figures 14(a) and 14(b).)

d. Wherein the asynchronous circuit is operable to sequentially control transmission

of the units of data in the pipelines such that the program order is maintained (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 17-37; column 12, line 55 to column 13, line 15; Figure 13; column 14, lines 53-61; Figure 14(b); column 15, lines 11-23 and 43-54; and Figure 15).

9. Claims 22 and 27 are substantially similar to claim 1 and rejection for the same reasons above. The only differences being that claim 22 is a computer-readable medium having data structures stored therein representative of claim 1 and claim 27 is a set of semiconductor processing masks.

10. Referring to claim 2, Vegesna has taught wherein the circuit comprises a processor (Vegesna column 1, lines 13-36) and wherein the N-way-issue resource comprises an instruction pipeline (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 27-37; column 12, line 55 to column 13, line 15; Figure 13; column 14, lines 53-61; Figure 14(b); column 15, lines 11-23; Figure 15; column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; and Figure 24).

11. Referring to claim 3, Vegesna has taught wherein N comprises an integer greater than 1 (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 27-37; column 12, line 55 to column 13, line 15; Figure 13; column 15, lines 11-23; Figure 15; column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; and Figure 24).

12. Referring to claim 4, Vegesna has taught an M-way-issue resource (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24), and interface circuitry operable to facilitate communication

between the N-way-issue resource and the M-way-issue resource (Vegesna column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

13. Referring to claim 5, Vegesna has taught wherein M is fewer than N (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

14. Referring to claim 6, Vegesna has taught wherein M is 1 and N is 2 (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

15. Referring to claim 7, Vegesna has taught wherein M is greater than N (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

16. Referring to claim 8, Vegesna has taught wherein M is 4 and N is 2 (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

17. Referring to claim 9, Vegesna has taught wherein the interface circuitry is operable to facilitate transmission of selected ones of the data units from the N-way-issue resource to the M-way issue resource (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

18. Referring to claim 10, Vegesna has taught wherein the interface circuitry is operable to facilitate transmission of selected ones of the data units from the M-way-issue resource to the N-way issue resource (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

19. Referring to claim 11, Vegesna has taught wherein the interface circuitry is operable to facilitate transmission of first selected ones of the data units from the N-way-issue resource to the M way-issue resource, and second selected ones of the data units from the M-way-issue resource to the N-way-issue resource (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

20. Referring to claim 12, Vegesna has taught wherein there is a one-to-one correspondence between the first and second selected data units (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

21. Referring to claim 13, Vegesna has taught wherein there is not a one-to-one correspondence between the first and second selected data units (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

22. Referring to claim 14, Vegesna has taught wherein the asynchronous circuit comprises a processor and wherein each of the N-way-issue resource and the M-way-issue resource comprises one of an instruction dispatcher, a register file, an instruction cache, a branch predictor, an instruction fetch circuit, a writeback circuit, an instruction decoding circuit, an execution pipeline, and branch circuitry (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

23. Referring to claim 20, Vegesna has taught wherein each pipeline comprises a plurality of stages, corresponding stages in each pipeline being interconnected in a state loop operable to communicate state information among the pipeline stages (Vegesna column 7, lines 13-28;

Figure 2; column 8, lines 27-37; column 12, line 55 to column 13, line 15; Figure 13; column 14, lines 53-61; Figure 14(b); column 15, lines 11-23; Figure 15; column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; and Figure 24).

24. Referring to claims 28, 44, and 49, Vegesna has taught a heterogeneous system for processing units of data having a program order associated therewith (Vegesna column 8, lines 17-26), the system comprising

a. An N-way issue resource and at least one multiple-issue resource having an order different from N (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24),

b. The N-way issue resource being operable to issue the units of data in N parallel pipelines staggered in time (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 17-37; column 12, line 55 to column 13, line 15; Figure 13; column 14, lines 53-61; Figure 14(b); column 15, lines 11-23 and 43-54; and Figure 15 – In regards to Vegesna, while the instructions are fetched simultaneously, the individual pipelines themselves control the issuance of the instructions and data, so there is only a possibility that the instructions will be issued by the individual pipelines simultaneously. The issuance of the instructions are dependent upon whether the dependency of the instruction is resolved or not, so an individual pipeline would stall an instruction's issuance to a later point in time when the instruction dependency has been resolved. Also, pipelines themselves stagger the issuance of instructions in individual pipelines, since the individual pipelines

issue its instructions at different points in time, as shown in Figures 14(a) and 14(b).)

c. The system further comprising interface circuitry operable to facilitate communication between the N-way-issue resource and the at least one multiple-issue resource (Vegesna column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24) and to preserve the program order in all of the resources (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 17-37; column 12, line 55 to column 13, line 15; Figure 13; column 14, lines 53-61; Figure 14(b); column 15, lines 11-23 and 43-54; and Figure 15).

25. Claims 44 and 49 are substantially similar to claim 28 and rejection for the same reasons above. The only differences being that claim 44 is a computer-readable medium having data structures stored therein representative of claim 28 and claim 49 is a set of semiconductor processing masks.

26. Referring to claim 29, Vegesna has taught wherein the at least one multiple-issue resource comprises a plurality of multiple-issue resources having different orders (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

27. Referring to claim 30, Vegesna has taught wherein the interface circuitry comprises a dispatch circuit operable to route the data units received from the N-way issue resource on a first number of input channels to designated ones of a second number of output channels associated with the at least one multiple-issue resource in a deterministic manner thereby preserving a partial ordering for each output channel defined by the program order (Vegesna column 19, lines

58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

28. Referring to claim 31, Vegesna has taught wherein the N-way issue resource comprises first and second pipelines (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 27-37; column 12, line 55 to column 13, line 15; Figure 13; column 15, lines 11-23; Figure 15; column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; and Figure 24), and the interface circuitry comprises a dual filter comprising a dual-issue input datapath corresponding to the first and second pipelines, a single-issue output datapath, and a control channel, the dual filter being operable to selectively transmit data tokens on the input datapath to the output datapath according to control information on the control channel (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

29. Referring to claim 32, Vegesna has taught wherein the interface circuitry comprises remapping circuitry operable to route the data units received from the at least one multiple-issue resource on a first number of input channels to designated ones of a second number of output channels associated with the N-way issue resource in a manner which preserves the program order (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

30. Referring to claim 34, Vegesna has taught wherein the at least one multiple-issue resource comprises an M-way issue resource where M is an integer multiple of N (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24), and wherein the interface circuitry comprises a plurality

of split circuits which operate alternately to transmit the data units from the N-way issue resource to the M-way issue resource, and a plurality of merge circuits which operate alternately to transmit the data units from the M-way issue resource to the N-way issue resource (Vegesna column 31, line 58 to column 33, line 35; Figure 19; Figure 27; and Figure 28).

31. Referring to claim 35, Vegesna has taught wherein the at least one multiple-issue resource comprises an M-way issue resource where M is less than N (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24), and wherein the interface circuitry comprises at least one optional assign circuit which is operable to receive the data units from both of the N-way issue resource and M-way issue resource and to selectively transmit the received data units back into the N-way issue resource, thereby mitigating effects of a difference in throughput between the N-way issue resource and the M-way issue resource (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

32. Referring to claim 37, Vegesna has taught wherein the at least one optional assign comprises first and second input datapaths, an output datapath, and a control input, the at least one optional assign being operable to transmit a first data token on the first input datapath to the output datapath when the control input is in a first state, the at least one optional assign further being operable to discard the first data token and to transmit a second data token on the second input datapath to the output datapath when the control input is in a second state (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

33. Referring to claim 38, Vegesna has taught wherein the at least one optional assign further being operable to discard the second data token and to transmit the first data token to the output datapath when the control input is in a third state (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

34. Referring to claim 39, Vegesna has taught wherein the interface circuitry comprises a dual repeat circuit comprising a single-issue data input channel, a dual-issue data output channel, and a control channel, the dual repeat circuit being operable in response to control information on the control channel to transmit a first data token on the input channel to the output channel and to maintain the first data token on the input channel for future use, the dual repeat circuit also being operable in response to the control information to transmit a second data token on the input channel to the output channel and to discard the second data token so that the input channel can receive subsequent data token (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

35. Referring to claim 40, Vegesna has taught wherein the N-way issue resource has N pipelines associated therewith, and wherein the at least one multiple-issue resource has P pipelines associated therewith, and wherein N may be any of fewer than P, equal to P, or greater than P (Vegesna column 7, lines 13-28; Figure 2; column 8, lines 27-37; column 12, line 55 to column 13, line 15; Figure 13; column 15, lines 11-23; Figure 15; column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; and Figure 24).

36. Referring to claim 41, Vegesna has taught wherein there is a one-to-one correspondence between the data units in the N-way issue resource and the data units in the at least one multiple-

issue resource (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

37. Referring to claim 42, Vegesna has taught wherein, at any given time, more of the data units are in the N-way issue resource than the at least one multiple-issue resource (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

Claim Rejections - 35 USC § 103

38. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

39. Claims 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al., U.S. Patent Number 5,488,729 (herein referred to as Vegesna), as applied to claims 1 and 4 above, and in view of Hinton et al., U.S. Patent Number 5,428,811 (herein referred to as Hinton). Vegesna has not taught

a. Wherein the interface circuitry is operable to identify selected ones of the data units in a higher order one of the resources for transmission to a lower order one of the resources (Applicant's claim 15).

b. Wherein the interface circuitry is operable to transmit selected ones of the data units generated by a lower order issue one of the resources to a higher order issue one of the resources in such a way as to facilitate preservation of the program order (Applicant's claim 16).

c. Wherein each pipeline is operable to transmit the units of data in accordance with an asynchronous handshake protocol (Applicant's claim 17).

d. Wherein the asynchronous handshake protocol between a sender and a receiver in each of the pipelines comprises (Applicant's claim 18):

i. The sender sets a data signal valid when an enable signal from the receiver goes high (Applicant's claim 18);

ii. The receiver lowers the enable signal upon receiving the valid data signal (Applicant's claim 18);

iii. The sender sets the data signal neutral upon receiving the low enable signal (Applicant's claim 18); and

iv. The receiver raises the enable signal upon receiving the neutral data signal (Applicant's claim 19).

e. Wherein the handshake protocol is delay-insensitive (Applicant's claim 19).

40. However, Vegesna has taught a multi-functional unit approach, dividing the functional units according to the number of cycles needed to complete an operation (Vegesna column 12, line 55 to column 13, line 15; Figure 13; column 14, lines 53-61; column 15, lines 11-22; and Figure 15). Hinton has taught a multi-functional unit, dividing the functional units according to the number of cycles needed to complete an operation (Hinton column 4, lines 15-29)

a. Wherein the interface circuitry is operable to identify selected ones of the data units in a higher order one of the resources for transmission to a lower order one of the resources (Applicant's claim 15) (Hinton Abstract; column 4, lines 8-29;

column 5, line 21 to column 6, line 64; column 7, lines 33-54; column 8, line 55 to column 10, line 28; Figure 1; and Figure 3).

b. Wherein the interface circuitry is operable to transmit selected ones of the data units generated by a lower order issue one of the resources to a higher order issue one of the resources in such a way as to facilitate preservation of the program order (Applicant's claim 16) (Hinton Abstract; column 4, lines 8-29; column 5, line 21 to column 6, line 64; column 7, lines 33-54; column 8, line 55 to column 10, line 28; Figure 1; and Figure 3).

c. Wherein each pipeline is operable to transmit the units of data in accordance with an asynchronous handshake protocol (Applicant's claim 17) (Hinton Abstract; column 4, lines 8-29; column 5, line 21 to column 6, line 64; column 7, lines 33-54; column 8, line 55 to column 10, line 28; Figure 1; and Figure 3).

d. Wherein the asynchronous handshake protocol between a sender and a receiver in each of the pipelines comprises (Applicant's claim 18):

i. The sender sets a data signal valid when an enable signal from the receiver goes high (Applicant's claim 18) (Hinton Abstract; column 4, lines 8-29; column 5, line 21 to column 6, line 64; column 7, lines 33-54; column 8, line 55 to column 10, line 28; Figure 1; and Figure 3);

ii. The receiver lowers the enable signal upon receiving the valid data signal (Applicant's claim 18) (Hinton Abstract; column 4, lines 8-29; column 5, line 21 to column 6, line 64; column 7, lines 33-54; column 8, line 55 to column 10, line 28; Figure 1; and Figure 3);

iii. The sender sets the data signal neutral upon receiving the low enable signal (Applicant's claim 18) (Hinton Abstract; column 4, lines 8-29; column 5, line 21 to column 6, line 64; column 7, lines 33-54; column 8, line 55 to column 10, line 28; Figure 1; and Figure 3); and

iv. The receiver raises the enable signal upon receiving the neutral data signal (Applicant's claim 19) (Hinton Abstract; column 4, lines 8-29; column 5, line 21 to column 6, line 64; column 7, lines 33-54; column 8, line 55 to column 10, line 28; Figure 1; and Figure 3).

e. Wherein the handshake protocol is delay-insensitive (Applicant's claim 19) (Hinton Abstract; column 4, lines 8-29; column 5, line 21 to column 6, line 64; column 7, lines 33-54; column 8, line 55 to column 10, line 28; Figure 1; and Figure 3).

41. A person of ordinary skill in the art at the time the invention was made would have recognized that the protocol of Hinton ensures that all data and register space necessary for an instruction to be executed and completed is available, thereby ensuring that an instruction can properly execute prior to issuing the instruction to the execution units. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the handshake protocol of Hinton in the device of Vegesna to ensure an instruction can properly be executed before issuing the instruction to the execution units.

42. Claims 21 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al., U.S. Patent Number 5,488,729 (herein referred to as Vegesna), as applied to claim 1 above, and in view of Ahlgren et al.'s "SiGe Comes of Age in the Semiconductor

Industry" ©08 July 2002 (herein referred to as Ahlgren). Vegesna has not taught wherein the asynchronous circuit or the system comprises any of a CMOS integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit. Ahlgren has taught the circuit or the system comprises any of a CMOS integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit (Ahlgren page 1, "Technology Overview"). A person of ordinary skill in the art at the time the invention was made, and as recognized by Ahlgren, would have recognized CMOS circuits more efficiently use power, GaAs circuits improves performance by boosting switching speed, and SiGe circuits provides a performance boost as well. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the CMOS, GaAs, and SiGe circuits of Ahlgren for power consumption efficiency and performance boosts.

43. Claims 23-26 and 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al., U.S. Patent Number 5,488,729 (herein referred to as Vegesna), as applied to claim 1 above, and in view of Bauer et al.'s "A Reconfigurable Logic Machine for Fast Event-Driven Simulation" ©1998 (herein referred to as Bauer). Vegesna has not taught

a. Wherein the data structures comprise a simulatable representation of the circuit or system (Applicant's claims 23 and 45).

b. Wherein the simulatable representation comprises a netlist (Applicant's claims 24 and 46).

c. Wherein the data structures comprise a code description of the circuit (Applicant's claims 25 and 47).

d. Wherein the code description corresponds to a hardware description language

(Applicant's claims 26 and 48).

44. Bauer has taught

a. Wherein the data structures comprise a simulatable representation of the circuit or system (Applicant's claims 23 and 45) (Bauer Abstract and Introduction, paragraphs 1-2 and 6).

b. Wherein the simulatable representation comprises a netlist (Applicant's claims 24 and 46) (Bauer Abstract; Netlist Generation, paragraph 1).

c. Wherein the data structures comprise a code description of the circuit (Applicant's claims 25 and 47) (Bauer Abstract and Introduction, paragraphs 1-2 and 6).

d. Wherein the code description corresponds to a hardware description language (Applicant's claims 26 and 48) (Bauer Abstract and Introduction, paragraphs 1-2 and 6).

45. A person of ordinary skill in the art at the time the invention was made and as taught by Bauer, would have recognized that the simulation system of Bauer increases the speed of event-driven behavioral simulation (Bauer Abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the simulator of Bauer in the device of Vegesna to increase simulator speed.

46. Claims 33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al., U.S. Patent Number 5,488,729 (herein referred to as Vegesna), as applied to claim 35 above, and in view of Murase et al., U.S. Patent Number 5,832,303 (herein referred to as Murase). Vegesna has taught

a. Wherein the remapping circuitry comprises a circuit which is controlled by routing information generated when the data units are transmitted from the N-way issue resource to the at least one multiple-issue resource (Applicant's claim 33) (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

b. Wherein the interface circuitry further comprises a circuit by which the data units are transmitted from the M-way issue resource to the at least one optional assign circuit (Applicant's claim 36) (Vegesna column 19, lines 58-62; Figure 18; column 23, lines 8-42; column 26, lines 3-49; column 27, line 33 to column 29, line 5; and Figure 24).

47. Vegesna has not taught the circuit is a crossbar circuit. Murase has taught a crossbar circuit (Murase column 1, lines 50-61; column 2, lines 29-45; column 2, line 66 to column 3, line 18; Figure 1; column 6, lines 20-51; and Figure 5). A person of ordinary skill in the art at the time the invention was made, and as taught by Murase, would have recognized that the crossbar switch reduces the number of signal lines while performing at higher speeds (Murase column 1, lines 50-54). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the crossbar of Murase in the device of Vegesna to perform high-speed interconnection switches while reducing the number of signal lines.

Response to Arguments

48. Applicant's arguments filed 12 January 2007 have been fully considered but they are not persuasive.

49. Applicants argue in essence on page 11 "...there is more than ample information provided in the present application to enable one of ordinary skill in the art to design and simulate the circuits and systems claimed..." This has not been found persuasive. As the Examiner pointed out in the rejection, there are hundreds, if not thousands, of methods and techniques to implement this device in simulatable representations. Applicants even admit this in their arguments ("...there are a wide variety of tools which facilitate the layout and design of such circuits..."). However, even if the choice of tools were driven by the particular design style, a person of ordinary skill in the art would have to perform an undue amount of experimentation to develop the invention described in the claims without further guidance by the Applicants. Even with the mentioning of specific well-known tools in the present specification, there is no guidance on how to use these tools to make the invention claimed. The purpose of a specification is to "contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same...". However, the specification contains no information on how to make the device using simulatable representations other than they can be used to make the invention. As such, the specification lacks "full, clear, concise, and exact terms as to enable" the device in simulatable representations. While simulatable representations are known in the art, this does not mean that it is known in the art how to enable and realize Applicants' exact invention in simulatable representations.

50. Applicants argue in essence on pages 12-13

> ...These amendments are supported in the present specification...and are clearly distinguishable from the system described in Vegesna which repeatedly stresses that a key aspect of its approach is that the instructions issued to its parallel pipelines are issued *simultaneously*...

51. This has not been found persuasive. The exact claim language added states, taking claim 1 as exemplary, "issuance of the data units in the respective pipelines being staggered in time". The added claim language merely calls for each pipeline to issue its data at different points in time. As pointed out in the rejection above, Vegesna teaches that, while the instructions are fetched from memory simultaneously, the individual pipelines themselves control the issuance of the instructions and data, so there is only a possibility that the instructions will be issued by the individual pipelines simultaneously. The issuance of the instructions are dependent upon whether the dependency of the instruction to be issued is resolved or not, so an individual pipeline would stall an instruction's issuance to a later point in time when the instruction dependency has been resolved. Also, pipelines themselves stagger the issuance of instructions in individual pipelines, since the individual pipelines issue its instructions at different points in time, as shown in Figures 14(a) and 14(b). Figures 14(a) and 14(b) shows that the two asynchronous pipelines actually issue their individual instructions at different points in time. For example, in Figure 14(b) the integer pipeline issues in the fetch stage an integer instruction while the floating-point pipeline issues a floating-point instruction at cycle 1. In cycle 2, each pipeline issues a second instruction associated with each pipeline. Therefore, each pipeline issues a data unit at a different point in time.

Conclusion

52. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Vegesna et al., U.S. Patent Number 5,640,588, has taught asynchronous pipelines that execute simultaneously fetched instructions.

b. Chamdani et al., U.S. Patent Numbers 6,112,019 and 6,311,261, have taught independent pipelines that have instructions that are sent simultaneously to each independent pipeline.

53. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

54. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

56. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

57. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J. Li
25 March 2007

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